



Faculty Development Program



VIT[®]
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Event Outcome

Title : System on Chip Design: From basics to applications

Date : 2025-12-01 - 2025-12-05

Time : 10:00 - 17:30

Venue : TT238

- Space optimization: Integrating multiple components into a single chip dramatically reduces the physical size of the final product, allowing for smaller and more portable devices
- Power efficiency: SoCs are more power-efficient because they eliminate the need for multiple separate chips and reduce the distance signals must travel, making them ideal for battery-powered devices.
- Performance improvement: By keeping signals on a single chip, SoCs achieve higher speeds and lower latency compared to multi-chip solutions
- Reduced cost: A single SoC can be cheaper to manufacture than a system using multiple separate chips, and lower power consumption also contributes to lower operating costs.
- Enabling advanced features: The integration of specialized components, such as dedicated graphics processing units (GPUs), AI accelerators, and various communication modems, allows SoCs to handle complex tasks like machine learning, video processing, and high-speed wireless communication.

	<p>Resource Person 1 - Details Name : Sri Adibhatla Sridevi Designation : Professor Grade 2, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 2 - Details Name : Kittur Harish Mallikarjun Designation : Professor Higher Academic Grade, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 3 - Details Name : Kumaravel S Designation : Professor Grade 1, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 4 - Details Name : Sivanantham S Designation : Professor Grade 2, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 5 - Details Name : Jagannadha Naidu K Designation : Associate Professor Grade 1, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 6 - Details Name : Nithish Kumar V Designation : Associate Professor Grade 2, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 7 - Details Name : Ravi S Designation : Associate Professor Grade 1, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>
	<p>Resource Person 8 - Details Name : Ragunath G Designation : Assistant Professor Sr. Grade 1, School of Electronics Engineering University/ Company : VIT, Vellore Address : India, 632014.</p>

**Resource Person 9 - Details****Name :** Rajeev Pankaj Nelapati**Designation :** Associate Professor Grade 1, School of Electronics Engineering**University/ Company :** VIT, Vellore**Address :** India, 632014.**Resource Person 10 - Details****Name :** Sakthivel R**Designation :** Professor Grade 2, School of Electronics Engineering**University/ Company :** VIT, Vellore**Address :** India, 632014.**Resource Person 11 - Details****Name :** Padmanaban K**Designation :** Sr Engineer, Intel**University/ Company :** Intel India, Bangalore**Address :** India, 560103.**Resource Person's Profile :****1. Profile of Sri Adibhatla Sridevi**

PROFESSOR

2. Profile of Kittur Harish Mallikarjun

Professor HAG

3. Profile of Kumaravel S

PROFESSOR

4. Profile of Sivanantham S

Professor

5. Profile of Jagannadha Naidu K

Associate Professor

6. Profile of Nithish Kumar V

ASSOCIATE PROFESSOR

7. Profile of Ravi S

ASSOCIATE PROFESSOR

8. Profile of Ragunath G

ASSISTANT PROFESSOR SENIOR

9. Profile of Rajeev Pankaj Nelapati

ASSOCIATE PROFESSOR

10. Profile of Sakthivel R

PROFESSOR

11. Profile of Padmanaban K

Sr Engineer - Intel India Bangalore

The term "for all" highlights that SoCs are now a dominant technology in almost all modern electronic devices, from wearables and appliances to automotive systems and IoT devices. This program aims to promote comprehensive FPGA prototyping and industry-standard ASIC design methodologies

Cadence EDA Tools

Coordinator's: Prof. RAVI S 11403 - Associate Professor Grade 1 - SENSE
Prof. SAKTHIVEL R 10540 - Professor Grade 2 - SENSE